ABSTRACT OF THE DISCLOSURE

An anti-starvation interrupt protocol for use in avoiding livelock in a multiprocessor computer system is provided. At least one processor is configured to include first and second control status registers (CSRs). The first CSR buffers information, such as interrupts, received by the processor, while the second CSR keeps track of the priority level of the interrupts. When an interrupt controller receives an interrupt, it issues a write transaction to the first CSR at the processor. If the first CSR has room to accept the write transaction, the processor returns an acknowledgement, whereas if the first CSR is already full, the processor returns a no acknowledgment. In response to a no acknowledgment, the interrupt controller increments an interrupt starvation counter, and checks to see whether the counter exceeds a threshold. If not, the interrupt controller waits a preset time and reposts the write transaction. If it does, the interrupt controller issues a write transaction having a higher priority to the second CSR. In response, the processor copies all of the pending interrupts from the first CSR into the memory subsystem, thereby freeing up the first CSR to accept additional write transactions.